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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER

MAI, TAN V

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/035,647	Applicant(s) STEELE, GUY L.	
	Examiner Tan V Mai	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/1, 3/223/27, 4/26 & 11/19/02, 6/15/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 7-37 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. The disclosure is objected to because of the following informalities:

In the specification, pages 1 and 11; the status of Co-pending Application(s) Serial No. _____ is required to be kept current.

Appropriate correction is required.

2. The abstract of the disclosure is objected to because legal phraseology is used in this paragraph (i.e., "comprises"). Correction is required. See MPEP § 608.01(b).

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14 and 18-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims recite a method for performing a mathematical function. The claimed invention comprises a plurality of mental steps whereby the claimed mental steps are non-statutory subject matter. Specifically, the claimed method steps can be practiced mentally in conjunction with pen and paper.

However, in order for such a claimed computer-related process to be statutory, the method claims must include either a step that results: (1) in a physical transformation outside the computer, (2) in a limitation to a practical application, or (3) performed specific machine/element(s). Accordingly, claims 14 and 18-25 are clearly directed to a non-statutory process.

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5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-5 and 7-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (Applicant's admission Prior Art).

As per independent claim 1, Huang et al disclose, e.g., see **Fig. 4**, the invention, **arithmetic calculation circuit (100)**, substantially as claimed, including: **X and Y operand registers 116 & 118; arithmetic section 114 and special operand generator 122**. It is noted that Huang et al do not specifically detail the claimed "analyzer circuit configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand ". However, Huang et al do disclose X and Y operand registers each includes a special operand indicator which is stored a special operand of a predetermine set of special operands. Therefore, the Huang et al's feature is equivalent to the claimed "determine a **first status** of a first floating point operand and a **second status** of a second floating point operand". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Huang et al's teachings because the device is an **arithmetic calculation circuit (100)** having special operand indicator in each operand register as claimed.

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As per dependent claim 2, the claim adds: (1) "first / second operand buffer" and (2) "first / second operand analysis circuit". First, the "operand buffer" feature is obvious to a person having ordinary skill in the art for temporary storing desired data. Second, Huang et al's arithmetic section 114 should have circuit(s) for determining the first / second status as claimed.

As per dependent claim 3, the claim adds the "first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer". Huang et al disclose the equivalent feature, i.e., "X and Y operand registers each includes a special operand indicator which is stored a special operand of a predetermine set of special operandsfeature".

As per dependent claim 4, the claim adds the "memory storage external ...is a floating point status register". The feature is well known in art for indicating the special floating point operands.

As per dependent claim 5, the claim details the "results circuit". Huang et al's arithmetic section 114 and special operand generator 122 are capable of providing the "resulting floating point operand and embed the resulting status" as claimed.

As per dependent claim 7, the claim adds the list of status. Huang et al disclose the equivalent feature, e.g., claim 3.

As per dependent claims 8-13, the claim adds the details of the status. These features are obvious design choice.

Due to the similarity of claims 14-37 to claims 1-5 and 7-13, they are rejected under a similar rationale.

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7. Claims 1-5 and 7-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al (Applicant's admission Prior Art).

As per independent claim 1, Lynch et al disclose, e.g., see **Fig. 4**, the invention, **floating point unit (36)**, substantially as claimed, including: **Register Stack (84)** and **FPU Core (94)**. It is noted that Lynch et al do not specifically detail the claimed "analyzer circuit configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand ". However, Lynch et al do disclose the equivalent function, e.g., see Abstract, "[b]y appending tag values to each floating point number, the floating point unit can quickly determine which floating point numbers are special floating point numbers and the type of special floating point number". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Lynch et al's teachings because the device is a **floating point unit (36)** having the "determine which floating point numbers are special floating point numbers and the type of special floating point number" as claimed.

As per dependent claim 2, the claim adds: (1) "first / second operand buffer" and (2) "first / second operand analysis circuit". First, the "operand buffer" feature is obvious to a person having ordinary skill in the art for temporary storing desired data. Second, Lynch et al's floating point unit (36), should have circuit(s) for determining the first / second status as claimed.

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As per dependent claim 3, the claim adds the "first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer". Lynch et al disclose the equivalent feature, i.e., "appends a tag value to each floating point number".

As per dependent claim 4, the claim adds the "memory storage external ...is a floating point status register". The feature is well known in art for indicating the special floating point operands.

As per dependent claim 5, the claim details the "results circuit". Lynch et al's floating point unit (36), is capable of providing the "resulting floating point operand and embed the resulting status" as claimed, e.g., see Fig. 6, element (144).

As per dependent claim 7, the claim adds the list of status. Lynch et al disclose the equivalent feature, e.g., col. 2, second complete paragraph.

As per dependent claims 8-13, the claim adds the details of the status. These features are obvious design choice.

Due to the similarity of claims 14-37 to claims 1-5 and 7-13 , they are rejected under a similar rationale.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

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9. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest the "wherein the adder logic circuit is organized according to the structure of a **decision table**" as recited in dependent claim 6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (703) 305-9761. The examiner can normally be reached on Tue-Fri from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned are:

Official (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



TAN V. MAI
PRIMARY EXAMINER